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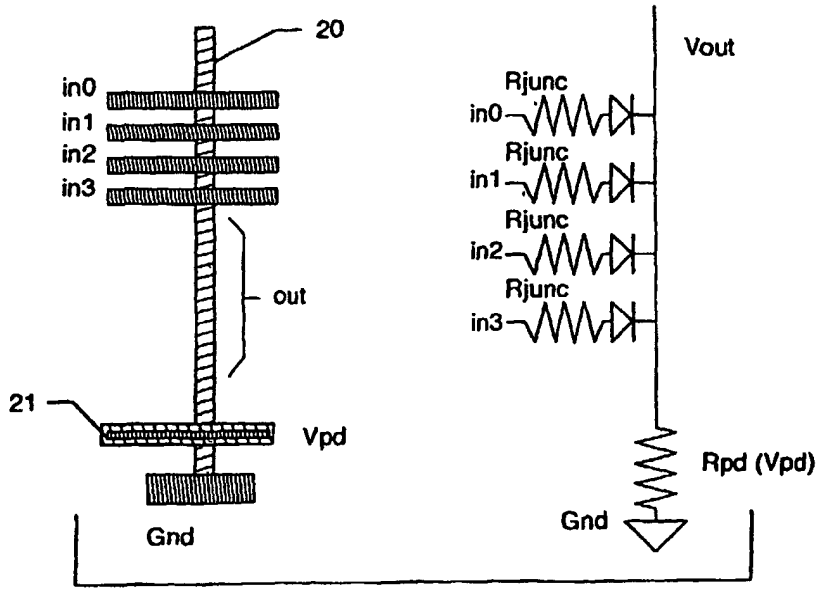
(54) Title: ARRAY-BASED ARCHITECTURE FOR MOLECULAR ELECTRONICS



(57) Abstract: An architecture for nanoscale electronics is disclosed. The architecture comprises arrays of crossed nanoscale wires having selectively programmable crosspoints. Nanoscale wires of one array are shared by other arrays, thus providing signal propagation between the arrays. Nanoscale signal restoration elements are also provided, allowing an output of a first array to be used as an input to a second array. Signal restoration occurs without routing of the signal to non-nanoscalewires.

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ARRAY-BASED ARCHITECTURE FOR MOLECULAR ELECTRONICS

Cross reference to related applications

[0001] This application claims the benefit of U.S. provisional Patent Application Serial Number 60/349,561, filed January 18, 2002 for a "Regular architecture for bootstrapping and operation of a universal, molecular-scale computing array" by Andre DeHon and Charles Lieber, the disclosure of which is incorporated herein by reference.

Statement regarding federally sponsored research or development

[0002] The present invention was made with support from the United States Government under Grant number N00014-01-0651 awarded by the Office of Naval Research of the Department of the Navy. The United States Government has certain rights in the invention.

BACKGROUND OF THE INVENTION

Field of the invention

[0003] The present invention relates to the field of sublithographic fabrication of electronic circuits, in particular molecular electronics. More specifically, an array-based architecture for molecular electronics is disclosed using a collection of techniques where small feature sizes are realized without lithographic processing. The arrays may be configured post-fabrication to implement any computable function of some finite size determined by the size of the arrays.

Description of the prior art

[0004] Today carbon nanotubes which are nanometers in diameter and microns long can be synthesized. See, for example, Cees Dekker, Carbon nanotubes as molecular quantum wires, Physics Today, pp. 22-28, May 1999. The growth and alignment of these nanotubes can be controlled, such that the nanotubes can be assembled into parallel rows of conductors and layered into arrays. See, for example, Yu Huang, Xiangfeng Duan, Qingqiao Wei, and Charles M. Lieber, Directed assembly of one-dimensional nanostructures into functional networks.

Ultimately, the nanotubes can be a single nanometer wide and spaced several nanometers apart.

[0005] At the same time, technologies to grow silicon nanowires are being developed. See, for example, Yi Cui, Lincoln J. Lauhon, Mark S. Gudiksen, Jianfang Wang, and Charles M. Lieber, Diameter-controlled synthesis of single crystal silicon nanowires, Applied Physics Letters, 78(15):2214-2216, 2001, and Alfredo M. Morales and Charles M. Lieber, A laser ablation method for synthesis of crystalline semiconductor nanowires, Science, 279:208-211, 1998. Also the silicon nanowires are only nanometers in width and can be grown or assembled into sets of long parallel wires. See, for example, Yong Chen, Douglas A. Ohlberg, Gilberto Medeiros-Ribeiro, Y. Austin Chang, and R. Stanley Williams, Self-assembled growth of epitaxial erbium disilicide nanowires on silicon(001), Applied Physics Letters, 76(26):4004-4006, 2000.. The electrical properties of these silicon nanowires can be controlled with dopants, yielding semiconductor wires, as shown, for example, in Yi Cui, Xiangfeng Duan, Jiangtao Hu, and Charles M. Lieber, Doping and electrical transport in silicon nanowires, Journal of Physical Chemistry B, 104(22):5213 5216, June 8, 2000.

[0006] It is also known how to build nanoscale crosspoints. Figure 1 is a schematic cross-sectional view which shows a suspended prior art nanotube conductor 1 coupled to a plurality of lower carbon nanotube or silicon nanowire conductors 2, 3, and 4 through a plurality of supports 5. The supports are made of a dielectric material, such as silicon dioxide. In this way, a nanotube-nanotube (or nanotube-nanowire) junction is formed. The junction is bistable with an energy barrier between the two states. In one state, see tubes 1-2 and 1-4, the tubes are "far" apart and mechanical forces keep the top wire 1 from descending to the lower wire 2, 4. At this distance the tunneling current between the crossed conductors is small, resulting, effectively, in a very high resistance (GigaOhms) between the conductors. In the second state, see tubes 1-3, the tubes come into contact and are held together via molecular forces. In this state, there is little resistance (about 100 KΩ) between the tubes. Therefore, by applying a voltage to the tubes, one can charge them to the same or opposite polarities and use

electrical charge attraction/repulsion to cross the energy gap of the junction between the two bi-stable states, effectively setting or resetting the programming of the connection. These junctions can be rectifying such that the connected state exhibits PN-diode rectification behavior. Molecular electronics PN-junctions are disclosed, for example, in Y. Cui and C.M. Lieber, "Functional Nanoscale Electronic Devices Assembled using Silicon Nanowire Building Blocks," Science 291, 891-893 (2001).

[0007] Also known in the prior art is how doped silicon nanowires can exhibit Field-Effect Transistor (FET) behavior. Figure 2 is a schematic perspective view of a prior art embodiment which shows oxide 10 grown over a silicon nanowire 11 to prevent direct electrical contact of a crossed conductor 12, for example a carbon nanotube or a silicon nanowire. The electrical field of one wire can then be used to "gate" the other wire, locally evacuating a region of the doped silicon nanowire of carriers to prevent conduction. FET resistance varies from Ohms to GigaOhms. Similarly, also carbon nanotubes can exhibit FET behavior. See, for example, Yu Huang, Xiangfeng Duan, Yi Cui, Lincoln Lauhon, Kevin Kim and Charles M. Lieber, "Logic Gates and Computation from Assembled Nanowire Building Blocks," Science, 2001, v294, p1313-1317, V. Derycke, R. Martel, J. Appenzeller and Ph. Avouris, "Carbon Nanotube Inter- and Intramolecular Logic Gates," Nano Letters, 2001,v1n9, p435-456, and Sander J. Trans, Alwin R.M. Verschueren and Cees Dekker, "Room-temperature Transistor Based on a Single Carbon Nanotube," Nature, 1998, v393, p49—51, May 7.

[0008] Furthermore, regular arrangements of nanoscale wires (parallel arrays of wires, crossed, orthogonal structures) are also known. A crossbar is usually defined as an array of switches that connect each wire in one set of parallel wires to every member of a second set of parallel wires that intersects the first set. Generally, the two sets of wires are perpendicular to each other. An interesting consequence of all these devices is the ability to store state and implement switching at a wire crossing. That is, the switch device itself holds its state. Therefore, crossbars in this technology can be fully populated with no cost in

density. This is particularly beneficial in achieving the necessary defect tolerance. See, for example, U.S. Pat. No. 6,256,767 to Kuekes and Williams.

[0009] The prior art also discloses how to build a wide range of electronic circuits where features at the scale of the device features (e.g. VLSI) can precisely be placed. Additionally, techniques for building universally programmable devices (e.g. PALs, PLAs, connections thereof) having VLSI fabrication capabilities are also known.

[0010] Recently, it is also known how to build small collections of non-restoring molecular scale logic and how to connect together non-restoring molecular scale logic at the microscale. See, for example, C.P. Collier, E. M. Wong, M. Belohradsky, F. M. Raymo, J. F. Stoddard, P. J. Kuekes, R. S. Williams, and J. R. Heath, "Electronically configurable molecular-based logic gates," Science, vol. 285, pp. 391-394, 1999.

[0011]Also known is an architecture based on molecular-scale electronic building blocks, called 'nanoFabrics.' See Seth Copen Goldstein and Mihai Budiu, "Nanofabrics: Spatial computing using molecular electronics," in Proceedings of the 28th Annual International Symposium on Computer Architecture, June 2001, pp. 178-189. However, the architecture disclosed in Goldstein is restricted to the use of two-terminal devices only and does not teach how nanoBlocks are customized.

[0012] It is still not known how to connect together large numbers of these nanoscale or sublithographic devices to create arbitrary logic functions. Additionally, it is still not known how to arrange for arbitrary connection of (cascading of) logic circuits at the nanoscale level without need for returning to a micro-scale level for signal restoration. It is also not known how to exploit the limited assembly techniques now possible to build arbitrary logic functions. It is also not known which logic structures are efficient when dealing with the cost constraints imposed by these fabrication techniques.

[0013] Throughout the present disclosure, the term micron-scale will refer to dimensions that range from about 0.1 micrometer to about 2 micrometers in size. The term nanometer-scale (also nanoscale) will refer to dimensions that range from 0.1 nanometers to 50 nanometers (0.05 micrometer), the preferred range being from 0.5 nanometers to 5 nanometers.

SUMMARY OF THE INVENTION

[0014] The present invention provides an architecture for molecular electronics based on carbon nanotubes and silicon nanowires. The architecture is based on a collection of interconnected arrays. The crossed arrays can act as memory elements (memory cores), computational elements (PLAs) and interconnecting elements (wires and crossbars). Further, the architecture according to the invention allows sparing and remapping to avoid defects in a base array. While a single, monolithic memory, PLA, or crossbar would not be useful or efficient, a collection of interconnected arrays as shown in the present invention will allow to both exploit logical structure and isolate faults.

[0015] According to a first aspect, an architecture for nanoscale electronics is provided, the architecture comprising: arrays of crossed nanoscale wires, each array comprising a plurality of crosspoints between nanoscale wires, the crosspoints being selectively programmable, wherein nanoscale wires of one array are shared by other arrays, thus providing signal propagation between the one array and the other arrays; and nanoscale signal restoration elements, allowing an output of a first array to be used as an input to a second array, wherein signal restoration occurs without routing of the signal to non-nanoscale wires.

[0016] According to a second aspect, a circuit is provided, comprising: a plurality of arrays having first and second sets of address lines and connections between the first and second sets of address lines; and a plurality of driving devices for the plurality of arrays, the driving devices having third and fourth sets of address lines and connections between the third and fourth sets of address lines, wherein the driving devices have a first condition in which they

act as decoders for the arrays, and a second condition in which they act as signal restoring devices for the arrays.

[0017] According to a third aspect, a method of driving a plurality of arrays having first and second sets of address lines and connections between the first and second sets of address lines is provided, the method comprising: providing a plurality of driving devices for the plurality of arrays, the driving devices having third and fourth sets of address lines and connections between the third and fourth sets of address lines, the driving devices having a first condition in which the driving devices act as decoders for the arrays, and a second condition in which the driving devices act as signal restoring devices for the arrays.

[0018] According to a fourth aspect, A method for assembly of arbitrary boolean logic computations at sublithographic scales is provided, the method comprising: providing sublithographic-scale arrays performing a predetermined logic function, such as a NOR logic function; interconnecting the arrays; and customizing the arrays to perform the logic function and signal routing.

[0019] The arrays can be either diode-based or FET-based. A diode-based array is a three dimensional array comprising a matrix of elements like those disclosed in Fig. 1. A FET based array is a three-dimensional array comprising a matrix of elements like those disclosed in Fig.2. Diode-based arrays can be alternated with FET-based arrays. Routing and signal polarity control is allowed by arrangement of overlap topologies and array inversions (e.g. OR and NOR).

[0020] The present disclosure will show in detail NOR arrays. Collections of NOR gates are universal, so this substrate is sufficient to perform any computation. Upon reading of the present disclosure, the person skilled in the art will be able to realize arrays based on a different kind of logic, e.g. NAND logic.

[0021] According to the present invention, uses and assembly techniques are advantageously disclosed to build a universal, programmable structure without

requiring signals to pass back from nanoscale to microscale for signal restoration. Additionally, key elements for micro-to-nanoscale interfacing are shown.

[0022] A further advantage of the present invention is that the architecture disclosed herein can provide universal logic functionality. The architecture allows a sufficient set of capabilities for performing logic, restoration, routing, and bootstrap programming using only large, crossed wire arrays.

[0023] Additional advantages of the architecture according to the present invention are its minimalism, defect tolerance, and compatibility with emerging, bottom-up, nanoscale fabrication techniques. Furthermore, the disclosed architecture also supports micro-to nanoscale interfacing for communication with conventional integrated circuits and bootstrap loading.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the drawings in which:

Figure 1 shows a schematic cross-sectional view of a prior art nanotube conductor;

Figure 2 shows a schematic perspective view of a prior art nanotube FET arrangement;

Figure 3 shows a nanotube wired-OR connection and its electrical equivalent;

Figure 4 shows a nanotube programmable diode OR array and its electrical equivalent;

Figure 5 shows a nanotube PFET NOR and its electrical equivalent;

Figure 6 shows a nanoscale decoder;

Figure 7 shows an example of a patterned decoder to be used with the present invention;

Figure 8 shows a schematic plan view of nanoscale arrays and encoders arranged in accordance with the present invention;

Fig. 9 shows a schematic view of the molecular electronics architecture according to the present invention;

Figure 10 shows an embodiment of the present invention where the decoders act also as a pull-up/pull-down circuit;
Figure 11 shows an arrangement of arrays forming a macro tile; and
Figure 12 shows how fabrication of additional wires in the array can avoid problems due to faulty wires and switches.

DETAILED DESCRIPTION OF THE INVENTION

Basic passive devices

[0025] Reference is initially made to Figure 3, the left side of which shows a nanotube wired OR logic arrangement. The right side of Figure 3 shows the electrical equivalent of the left side arrangement. The upper nanotubes or nanowires IN0, IN1, IN2, IN3 contact the lower nanotube 20, thus forming a plurality of low resistance PN-type junctions of the kind already discussed in Fig. 1. In case an upper nanotube INi is "far" from the lower nanotube 20, a high impedance configuration is formed. Element 21 is a nanotube covered by oxide, which presents a FET behavior (see Fig. 2), thus producing a voltage-controlled resistance value Rpd. Element 21 acts as a static load in the wired-OR arrangement shown in the Figure.

[0026] Figure 4 shows a programmable diode OR array. As usual, the left side shows the nanotube arrangement, and the right side shows the corresponding electrical equivalent. The black squares between upper nanotubes IN0..IN3 and lower nanotubes 30, 31 indicate that the upper nanotubes are suspended in the OFF position (see, for example, nanotubes 1-2 and 1-4 in Fig. 1). Therefore, upper nanotube IN0 does not contact lower nanotubes 30, 31; upper nanotube IN1 contacts lower nanotubes 30, 31; upper nanotube IN2 does not contact lower nanotube 30 and contacts lower nanotube 31; and upper nanotube IN3 contacts lower nanotube 30 and does not contact lower nanotube 31. Element 32 is a nanotube covered by oxide, which presents a FET behavior, thus producing a voltage-controlled resistance value Rpd, and acting as a static load.

Signal restoration

[0027] Both devices shown in Figure 3 and Figure 4 do not produce gain. Therefore, restoring logic performing signal restoration is needed to provide gain, either at the microscale or at the nanoscale level. Signal restoration allows high signals to be driven higher and low signals to be driven lower, in order to allow an arbitrary number of devices to be cascaded together and a logical distinction between a low logical value and a high logical value to be maintained. Therefore, signal restoration helps protecting the circuit against noise and allows arbitrary circuit composition.

[0028] According to the present invention, restoring logic is provided at the nanoscale level in order to allow the output of a first stage to be used as input for a second stage, making it possible to compute through an arbitrary number of logic stages without routing the signal to non-nanoscale (e.g., microscale) wires. In particular, FET devices of the kind shown in Fig. 2 will allow to define a restoring logic discipline at the nanoscale level. Using the FET junctions like those shown in Figure 2, NMOS-like inverters, NAND, AND, NOR, or OR logic can be built. For clarity purposes, the present application will focus on the electrical operation of the restoring FET NOR stage using p-type silicon nanowires and a PMOS-like logic discipline. Using only NOR arrays is sufficient to achieve universal logic. The person skilled in the art will also be able to realize embodiments for n-type silicon nanowires.

[0029] Figure 5 shows a nanotube PFET (p-type FET) NOR circuit and its electrical equivalent. In a first scenario (pull-up), all inputs IN0, .., INM-1of the FETs are low. As a consequence, there is conduction through all the FETs formed at the wire crossings (no evacuation of charge). Since there is conduction through all the FETs and the top end of the series of FETs is connected to a power supply driven to a high voltage, the wire can be pulled up to the high voltage of the power supply. The output is now high. In a second scenario (pull-down), one of the inputs IN0, .., INM-1 is high. Ideally, there is no conduction through the portion of the wire under this FET. This breaks the path from the high voltage supply to the output region of the wire. In absence of current flow,

the output cannot be pulled up to the high voltage. The static pulldown is always weakly enabled. If it is not pulling against a strong connection to the high voltage supply, as in the previous scenario, the weak static pulldown will be able to pull the output down to a low voltage level. The output of the FET is now low.

[0030] Alternatively, restoration at the nanoscale level could also be obtained by means of precharge logic structures. In the simplest case, the static pull-down in the NOR is replaced with a precharge gate. In fact, the same structure shown in Fig. 5 may serve this role as long as the pull-down gate is appropriately controlled. Alternatively, the single pull-down line could be microscale instead of nanoscale. Additionally, an additional microscale input to disable the pull-up could be added. Operation is started by driving the new pull-up line (the additional input) to a high value (disabling current flow to the power supply), and enabling the pull-down precharge line by driving it to a low value. This will allow the output to charge to a low value. After the output is charged to a low value, the pull-down is disabled. The output will remain at the low value for which it is now precharged. Subsequent to this, the new pull-up line is enabled. If all of the inputs are low, conduction is allowed to the power supply and the output can be pulled up. If one or more of the inputs are high, there is no such path and the output remains at a low voltage level. Thus, the device continues to perform its NOR function. Alternate stages will use complementary precharge phases, in order not to release the pull-up enable line while the inputs to a stage are still precharging and have not been allowed to evaluate. This domino-style logic technique is well-known per se in the prior art and will not be here explained in detail.

Bootstrapping

[0031] Once each of the crosspoints in each of the arrays is able to be programmed, the arrays are able to perform any desired logic or routing function. The personalization that allows arbitrary functions to be built is obtained through programming of the arrays. This is obtained by bootstrapping the process, i.e. by providing a starting logic which allows selective programming of the crosspoints of the arrays.

In particular, a large number of lines can be controlled by a relatively minor number of control lines by means of decoders. In this way, the crosspoints forming the arrays will be programmable, by means of the nanoscale decoder, to either connect (diode) or gate (FET) the nanoscale wires forming the crosspoints. The crosspoints will be programmable to exhibit a bi-stable behavior. For example, a first state of the crosspoints could correspond to a weak conductance state and a second state of the crosspoints could correspond to a strong conductance state between the nanoscale wires forming the crosspoints. Alternatively, a first state of a crosspoint could correspond to the first nanoscale wire of the crosspoint controlling the second nanoscale wire of the crosspoint, and a second state of the crosspoint could correspond to the first nanoscale wire of the crosspoint not controlling the second nanoscale wire of the crosspoint.

[0032] The architecture according to the present invention is based on a plurality of array cells. Therefore, power supply gating crossbars acting as decoders will be needed to allow a small number of microscale wires to connect to a larger number of nanoscale wires forming the array grids. In particular, the crossbars will have a set of crossed nanoscale wires. A first set of the nanoscale wires will be connected to a power supply and a second, orthogonal, set of nanoscale wires will control the resistance along the first set of wires. Figure 6 shows a nanoscale decoder block 60 on the edge of a nanowire array, not shown in the Figure. The decoder has N nanowires 64 (four in the figure) which connect to the nanowire array and $2 \log_2(N) + 1$ nanowires 65 (five in the figure) which connect to an orthogonal set of microscale wires 62 through nanovias 63. The extra control line 66 (the +1 in wires 65) is an enable line used to enable/disable the decoder connection. As usual, black squares in the decoder show OFF positions, allowing a unique address to be assigned to each of the nanoscale wires 64 of the decoder. Fig. 6 also shows a horizontal microscale wire 61 connected to the supply voltage. The microscale wire 61 is a source for the driving voltages in the array, i.e. one of the power supply lines for the circuit.

[0033] However, while address lines which are connected directly to the microscale wires 62 can be driven to a voltage by conventional electronics, it is

not possible to drive the nanoscale wires 64 which drive into the nanowire array. To address this, the decoder pattern can be customized during fabrication. An example of this customization in shown in Figure 7, where a customized decoder 60 is shown, obtained through a stamping process, as disclosed in Stephen Y. Chou, Peter R. Krauss, Wei Zhang, Lingjie Guo, and Lei Zhuang, "Sub-10 nm imprint lithography and applications," Journal of Vacuum Science and Technology B, vol. 15, no. 6, pp. 2897-2904, November-December 1997.
In particular, a predetermined pattern of blocks between the orthogonal layers of wires connecting to the nanowire array and to the microscale wires is imprinted. Where the pattern leaves openings, the two layers are allowed to contact, producing a strongly coupled FET arrangement. See, for example, location 70 in Figure 7. Where the blocks prevent the crossed wires from contacting, the crossed nanowires are far enough apart that they do not control each other. In a preferred embodiment, sparse encoding will be used, i.e. the decoder will be provided with additional encoding lines, in order to guarantee that a faulty address line will still allow proper operation of the decoder or will render only a small fraction of the array unaccessible. For example, a two-hot coding scheme can be considered, where every nanowire 64 is enabled by ANDing together a pair of address wires. Therefore, the patterning of the decoder does not need to be perfect, because it will always be possible, in the preferred embodiment, to tolerate not being able to address a small fraction of the nanoscale wires.

[0034] The decoders are then placed on either side of a nanoscale array, both in a horizontal and a vertical dimension, as shown in the schematic plan view of Fig. 8. Fig. 8 shows decoders 81-84 and an array 85, together with vertical nanowires 86, horizontal nanowires 87, vertical microwires 88, and horizontal microwires 89. The microwires feed the signals PUEN (pull-up enable), PDEN (pull-down enable), /A2, A2, /A1, A1, /A0, A0 (where the symbol /Ai is used to represent the complement of Ai) to the decoders 81, 82, 83, and 84. Ground voltage and supply voltage are provided through the lines GND and VDD. Using the decoders 81, 82, 83 and 84 of Figure 8, it is now possible to drive any single horizontal or vertical nanotube/nanowire to a high or low voltage, and leave the other nanotubes/nanowires floating. For example, a tube can be driven high by

driving all of the PFET nanowire crossings in the decoder low (i.e. the pull-up enable PUEN and all the address lines necessary to select this tube). In this way, a low impedance path from the tube to the high voltage supply will be generated. Assuming the pull-down enable PDEN is driven with a high voltage so that it is in high impedance mode, and the true and complement address lines Ai are driven with appropriately opposing voltages, only the selected line is driven and all the other lines are left to float to high-impedance. A tube can be driven low in a similar manner by driving the pull-up enable PUEN high and the pull-down enable PDEN low.

[0035] It can be noted that the embodiment of Figure 8 discloses four decoders for a single array. Alternative embodiments can also provide for the presence of two decoders only, a first decoder on an end of a horizontal run and a second decoder on an end of a vertical run. Decoders should be present on both horizontal and vertical wires in order to allow each crosspoint to be programmed by means of a voltage difference. In particular, in order for a crosspoint to be programmed, both the horizontal and the vertical line associated with that crosspoint will need to be driven. In the embodiment of Fig. 8, decoders are present at both ends of each horizontal or vertical wire run, in order to allow the lines to be pulled both high and low.

[0036] Figure 9 shows a schematic view of an operational computing system embodying the molecular electronics architecture according to the present invention. The architecture comprises:

1) A plurality of array cells 201, 202, 203, 204. In the example of the Figure, the arrays 201, 204 perform operations under an OR logic, and the arrays 202, 203 perform operations under a NOR logic. The array cells 201-204 are formed by crossed nanowires. For example, the array cell 201 is formed by crossed nanowires 210 and 212; the array cell 202 is formed by crossed nanowires 210 and 213; the array cell 203 is formed by crossed nanowires 211 and 212; and the array cell 204 is formed by crossed nanowires 214 and 215;

2) A plurality of driving devices 220-227 for the array cells 201-204; and

3) A plurality of microscale wires 205, 206 for transmitting input signals to the decoders 220-227 in order to program the crosspoints in the crossbar and to connect or disconnect the array from the logic power supplies.
4) A plurality of nanometer-scale signal restoration elements, like, for example, the NOR circuit shown in Fig. 5. The signal restoration elements restore the output signal of an array, allowing each signal to be correctly used as an input to a further array.

[0037] Therefore, according to the present invention, the nanoscale wires are arranged into interconnected, crossed arrays with non-volatile switching devices at their crosspoints. The crossed arrays can function as programmable logic arrays and programmable interconnect, as later explained in more detail.

[0038] It should be noted that during normal operation, the driving devices or decoders should not drive the nanoscale wire arrays. Rather, the nanoscale wire arrays will be performing logic of their own. Isolation of an array from a decoder will be obtained by driving both the pull-up enables and pull-down enables high.

[0039] Should the elements of the driving device be made of FET junctions like those shown in Fig. 2, such FETs could serve as a static pull-down/pull-up load (of the type already shown in Fig. 5) during operation, as shown in Figure 10. Figure 10 shows a nanoscale arrangement (left side) and its equivalent logical circuit (right side) in the simplified case of a single NOR array 92 made of PFETs. The decoding FETs 90, 91 are placed in series between the contact resistance Rc and the outputs 94 of the array 92. The outputs 94 of the array 92 are indicated as Vout in the electrical right side equivalent. By driving all of the horizontal address lines of the decoding FETs 90, 91 low, the programming FETs of the decoders 90, 91 will act as wires. Additionally, if the pull-up enable PUEN line of decoder 90 is driven low and the pull-down enable PDEN line of decoder 91 is driven with Vpd, the behavior of the circuit becomes substantially similar to the behavior of the NOR pull-up circuit of Figure 5, with the PDEN FET serving as

Rpd. A pull-down behavior will be obtained by driving the pull-up enable PUEN line with Vpd and by driving the pull-down enable PDEN line low.

[0040] Therefore, the power supply gating crossbars could act as open circuits, as low resistance devices, as controllable resistance devices, as a static pull-up/pull-down or as a precharge or evaluate gate during operation of the arrays.

[0041] As already noted, the output of the array 92 appears on the nanowires 94. To use the information on the nanowires 94 as subsequent input to another stage of logic, a further array 93 can be arranged orthogonal to the array 92. In this way, the input of the array 93 will align with the output of the array 92. The array 93 is orthogonal to the array 92 because the inputs 94 of the array 93 are vertical, and the outputs 96 of the array 93 are horizontal, differently from the array 92, where the inputs 95 are horizontal and the outputs 94 are vertical.

[0042] Fig. 11 shows an arrangement of sixteen different arrays forming a 4 x (2 x 2) macro tile. Macro-scale wires have been omitted to simplify the diagram. This arrangement allows inputs to enter from either side of the NOR-plane and outputs to depart in either orthogonal direction. Lines 101, 102, 103, and 104 show inputs to the macro tile. Lines 105, 106, 107, and 108 show outputs from the macro tile. For example, the vertical input signal 101 could be processed by the arrays 110, 111 under control of the decoders 114, 115, then horizontally input to the arrays 112, 113 under control of the decoders 117, 118, and finally output as horizontal output signal 105. The macro tile can be abutted horizontally and vertically to allow arbitrary Manhattan routing within the master array. Manhattan routing is a routing scheme in which connections are made on a rectilinear grid and signals are allowed to make only 90 degree turns at specified intersections.

[0043] In more complex configurations, diode-based arrays can be alternated with FET-based arrays. If only the diode-arrays are programmable, imprinting can be used to pattern fixed-connectivity NOR stages to provide both logic and signal restoration, realizing a PAL-like logic structure.

Ideally, the FET restoring logic should be programmable after fabrication, so that NOR stages can be first built and then programmed. However, at the present time, it is uncertain whether programmable FET junctions can be obtained.
What can be done is that of pairing non-restoring stages (e.g. diode stages) with restoring stages (e.g. FET stages). In this case, the whole device can be programmable even if the restoring stage itself is not programmable. In order to allow this embodiment to work properly, care must be taken in ensuring that the restoring stage can tolerate the signal loss associated with the non-restoring stage or stages and produce a restored signal which can properly drive the next non-restoring stage. For example, a restoring inverter stage could be placed between non-restoring programmable stages. Alternatively, the restoring stage may perform logic as well (e.g. NOR). Programmable devices which alternate a programmable stage followed by a non-programmable stage are well known in VLSI (e.g. PALs, which comprise a programmable OR plane followed by a fixed AND plane). Therefore, a structure with a non-restoring, programmable diode OR plane followed by a restoring, non-programmable FET NOR plane can be adopted. The non-programmable FET NOR can be defined during fabrication using similar techniques as used for the decoder (e.g. stamping).

[0044] According to the present invention, signal polarity control is obtained through arrangement of array inversions. For example, the NOR arrangement shown in Fig. 5 could be rotated upside-down, so that the static load (or precharge) Vpd is on top, the output in the middle , and the programmable crossbar inputs IN0 ..INM-1 are on the bottom, connecting the output to the low power supply, so that the function performed would be an OR instead of a NOR. Using a routing like the one shown in Fig. 11, a vertical composition can be obtained such that the array above the current array is a NOR array and the array below the current array is an OR array, so that the output of the current array can follow either an OR or a NOR logic. Therefore, if the outputs of the OR and NOR arrays can be routed back to the same array (for example the same starting array), then inversion of signals can be selectively controlled by choosing to route through the top (NOR) or bottom (OR) connected array.

[0045] When assembled into arrays, some of the nanoscale wires could have poor or non existent contacts, and individual switches might be non-functional. The architecture according to the present invention is designed to tolerate these defects by both local wire sparing and array sparing, where some of the arrays will be designated as spares. There is no logical significance to which wire is used to collect the output of a logical OR or NOR function. As long as the wires fabricated in the array are more than the wires actually needed, the faulty wires and switches can be avoided and logical operations can be performed on the functional wires. The base array size and the level of sparing included in the array are picked based on the specific defect rate expected at any point in time, similarly to the way spare rows and columns are designed in conventional DRAM memories. If the number of faulty components in some arrays or decoders exceeds the designed level of sparing, those arrays can be discarded. Multiple independent paths through different arrays in the design allow complete routing around faulty arrays.

[0046] Figure 12 shows, for example, how fabrication of additional wires in the array can avoid problems due to faulty wires and switches. In figure 12, numeral 120 shows a PLA in original logic, while numeral 130 shows an equivalent PLA with a faulty input 131 along line 132 and faulty inverter connections 133, 134 along lines 135, 136.

[0047] While several illustrative embodiments of the invention have been shown and described in the above description, numerous variations and alternative embodiments will occur to those skilled in the art. Such variations and alternative embodiments are contemplated, and can be made without departing from the scope of the invention as defined in the appended claims.

CLAIMS:

1.

An architecture for nanoscale electronics comprising:

arrays of crossed nanoscale wires, each array comprising a plurality of crosspoints between nanoscale wires, the crosspoints being selectively programmable, wherein nanoscale wires of one array are shared by other arrays, thus providing signal propagation between the one array and the other arrays; and

nanoscale signal restoration elements, allowing an output of a first array to be used as an input to a second array, wherein signal restoration occurs without routing of the signal to non-nanoscale wires.

2.

The architecture of claim 1, wherein the crosspoints are programmable to connect the nanoscale wires forming the crosspoints.

3.

The architecture of claim 1, wherein the crosspoints are programmable to gate the nanoscale wires forming the crosspoints.

4.

The architecture of any one of the previous claims, further comprising nanoscale driving devices of crossed nanoscale wires for the arrays, the crosspoints being programmable by means of the nanoscale driving devices.

5.

The architecture of claim 1, further comprising power supply gating crossbars having a set of crossed nanoscale wires, wherein a first set of nanoscale wires is connected to a power supply and a second, orthogonal, set of nanoscale wires controls resistance along the first set of nanoscale wires.

6.
The architecture of claim 4, further comprising non-nanoscale wires transmitting input signals to the driving devices.

7.
The architecture of claim 6, wherein the non-nanoscale wires are microscale wires.

8.
The architecture of claim 1, wherein the crosspoints are programmable to exhibit a bi-stable behavior.

9.
The architecture of claim 8, wherein a first state of the crosspoints corresponds to a weak conductance state and a second state of the crosspoints corresponds to a strong conductance state between the nanoscale wires forming the crosspoints.

10.
The architecture of claim 8, wherein a crosspoint consists of a first nanoscale wire crossed with a second nanoscale wire, a first state of the crosspoint corresponding to the first nanoscale wire controlling the second nanoscale wire, and a second state of the crosspoint corresponding to the first nanoscale wire not controlling the second nanoscale wire.

11.
The architecture of claim 10, wherein, in the first state of the crosspoint, voltage on the first nanoscale wire controls conductance through the second nanoscale wire.

12.
The architecture of any one of the previous claims, wherein the crosspoints comprise diode-type crosspoints.

13.

The architecture of any one of the previous claims, wherein the crosspoints comprise FET-type crosspoints.

14.

The architecture of claim 13, wherein the FET-type crosspoints are programmed during fabrication.

15.

The architecture of claim 14, wherein programming of the FET-type crosspoints is obtained through selective stamping.

16.

The architecture of claim 12, wherein programming of at least a portion of the crosspoints is performed after fabrication.

17.

The architecture of claim 16, wherein said programming is performed electrically.

18.

The architecture of claim 13, wherein programming of at least a portion of the crosspoints is performed after fabrication.

19.

The architecture of claim 18, wherein said programming is performed electrically.

20.

The architecture of any one of the previous claims, wherein the nanoscale signal restoration elements comprise arrays having FET-type crosspoints.

21.

The architecture of claim 20, wherein arrays having non-restoring logic elements are connected to arrays with signal restoring elements, such that a nanoscale restoring logic is obtained.

22.

The architecture of claim 5, wherein the power supply gating crossbars act as open circuit during operation of the arrays.

23.

The architecture of claim 5, wherein the power supply gating crossbars act as a low resistance device during operation of the arrays.

24.

The architecture of claim 5, wherein the power supply gating crossbars act as a controllable resistance device during operation of the arrays.

25.

The architecture of claim 5, wherein the power supply gating crossbars act as a static pull-up during operation of the arrays.

26.

The architecture of claim 5, wherein the power supply gating crossbars act as a static pull-down during operation of the arrays.

27.

The architecture of claim 5, wherein the power supply gating crossbars act as a precharge or evaluate gate during operation of the arrays.

28.

The architecture of any one of the previous claims, wherein a logical signal produced as output in one array is switched through the nanoscale wires and crosspoints to become an input to another array.

29.
The architecture of any one of the previous claims, wherein arbitrary signal routing is provided.

30.
The architecture of claim 29, wherein the arbitrary signal routing is provided by means of a Manhattan routing.

31.
The architecture of claim 29 or 30, wherein arrays performing logic functions and signal restoration also perform switching to enable routing.

32.
The architecture of any one of the previous claims, wherein signal polarity control is obtained through arrangement of array inversions.

33.
The architecture of any one of the previous claims, further comprising means for interfacing with non-nanoscale inputs and outputs.

34.
The architecture of any one of the previous claims, wherein the nanoscale wires comprise silicon nanowires.

35.
The architecture of any one of the previous claims, wherein the nanoscale wires comprise carbon nanotubes.

36.
The architecture of any one of the previous claims, wherein the nanoscale wires comprise silicon nanowires and carbon nanotubes.

37.

The architecture of any one of the previous claims, wherein defects in the architecture are avoided by post fabrication configuration.

38.

The architecture of claim 5, wherein the power supply gating crossbars have a first condition in which they selectively drive internal lines of core arrays, and a second condition in which they provide a connection to the power supply in order to enable the signal restoration elements.

39.

The architecture of any one of the previous claims, wherein the nanoscale wires comprise a first set of nanoscale wires having an oxide cover and a second set of nanoscale wires not having an oxide cover.

40.

The architecture of claim 39, wherein each wire crossing between a nanometer-scale wire of the first set of nanometer-scale wires and a nanometer-scale wire of the second set of nanometer-scale wires is able to exhibit a Field-Effect-Transistor (FET) behavior.

41.

The architecture of claim 5, wherein the power supply crossbars serve as decoders allowing selective addressing of individual array wires.

42.

The architecture of claim 41, wherein the selective addressing is used to program individual array crosspoints.

43.

The architecture of claim 42, wherein programming of individual array crosspoints is used to define the logic functionality of the array.

44.

The architecture of claim 42, wherein programming of individual array crosspoints is used to define routing of signals among arrays.

45.

The architecture of claim 42, wherein programming of individual array crosspoints allows arrays to be programmed to avoid defective components.

46.

The architecture of claim 41, wherein the decoders are provided with additional encoding lines.

47.

The architecture of claim 41, wherein each decoder comprises N nanoscale wires connected with the arrays and $2\log_2(N)$ +1 nanoscale wires connected with non-nanoscale wires.

48.

The architecture of claim 41, wherein the decoders comprise a decoder pattern, the decoder pattern being customized during fabrication of the decoders.

49.

The architecture of any one of the previous claims, wherein the arrays comprise a first array and a second array, the first array having an output and the second array having an input, wherein the output of the first array is the input of the second array and wherein the second array is placed orthogonally to the first array.

50.

The architecture of any one of the previous claims, wherein the arrays further include spare arrays.

51.

The architecture of any one of the previous claims, wherein faulty arrays are avoidable by signal routing through the arrays.

52.

The architecture of any one of the previous claims, wherein faulty arrays are avoidable by post fabrication configuration of signal routing through the array.

53.

The architecture of any one of the previous claims, wherein one or more of the arrays serve as memory arrays.

54.

A circuit comprising:

a plurality of arrays having first and second sets of address lines and connections between the first and second sets of address lines; and

a plurality of driving devices for the plurality of arrays, the driving devices having third and fourth sets of address lines and connections between the third and fourth sets of address lines,

wherein the driving devices have a first condition in which they act as decoders for the arrays, and a second condition in which they act as signal restoring devices for the arrays.

55.

A method of driving a plurality of arrays having first and second sets of address lines and connections between the first and second sets of address lines, the method comprising:

providing a plurality of driving devices for the plurality of arrays, the driving devices having third and fourth sets of address lines and connections between the third and fourth sets of address lines, the driving devices having a first condition in which the driving devices act as decoders for the arrays, and a second condition in which the driving devices act as signal restoring devices for the arrays.

56.

A method for assembly of arbitrary boolean logic computations at sublithographic scales, the method comprising:

providing sublithographic-scale arrays performing a predetermined logic function;

interconnecting the arrays; and

customizing the arrays to perform the logic function and signal routing.

57.

The method of claim 56, wherein the arrays are cascaded through sublithographic interconnections.

58.

The method of claim 56 or 57, wherein the logic is programmable after fabrication.

59.

The method of any one of claims 56 to 58, wherein the signal routing is programmable after fabrication.

60.

The method of any one of claims 56 to 59, wherein portions of the logic are specified during fabrication.

61.

The method of any one of claims 56 to 60, wherein portions of the routing are specified during fabrication.

62.

The method of any one of claims 56 to 61, wherein the logic is tolerant to defects in assembly.

63.

The method of any one of claims 56 to 61, wherein the logic is programmable after fabrication to tolerate defects in assembly.

64.

The method of any one of claims 56 to 63, wherein signal routing is programmable after fabrication to tolerate defects in assembly.

* * *

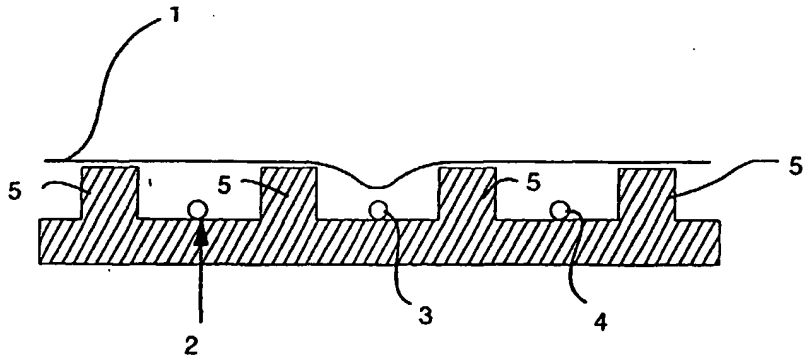


FIG. 1
PRIOR ART

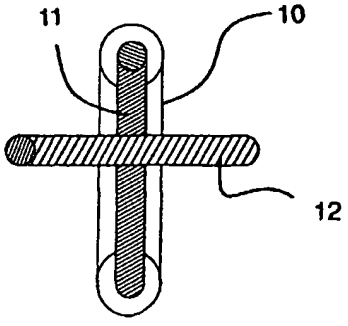
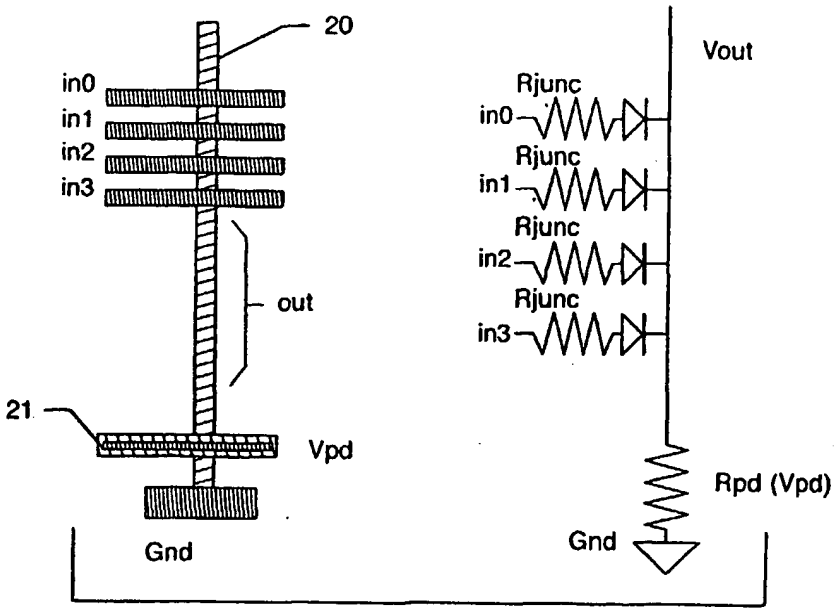


FIG. 2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in0
in1
in2
in3
out
21
Vpd
Gnd
Vout
Rjunc
in0
Rjunc
in1
Rjunc
in2
Rjunc
in3
Rpd (Vpd)
Gnd

FIG. 3

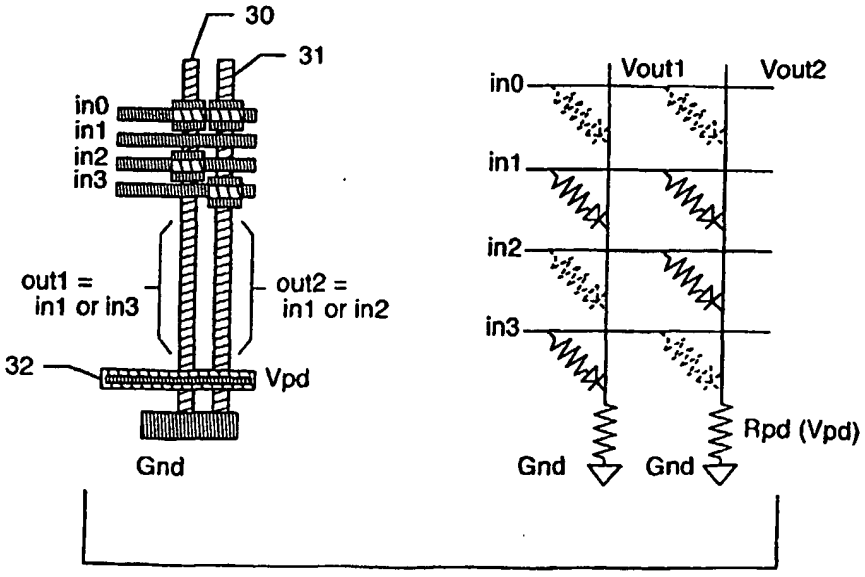
30
31
in0
in1
in2
in3
out1 =
in1 or in3
out2 =
in1 or in2
32
Vpd
Gnd
Vout1
Vout2
in0
in1
in2
in3
Rpd (Vpd)
Gnd
Gnd

FIG. 4

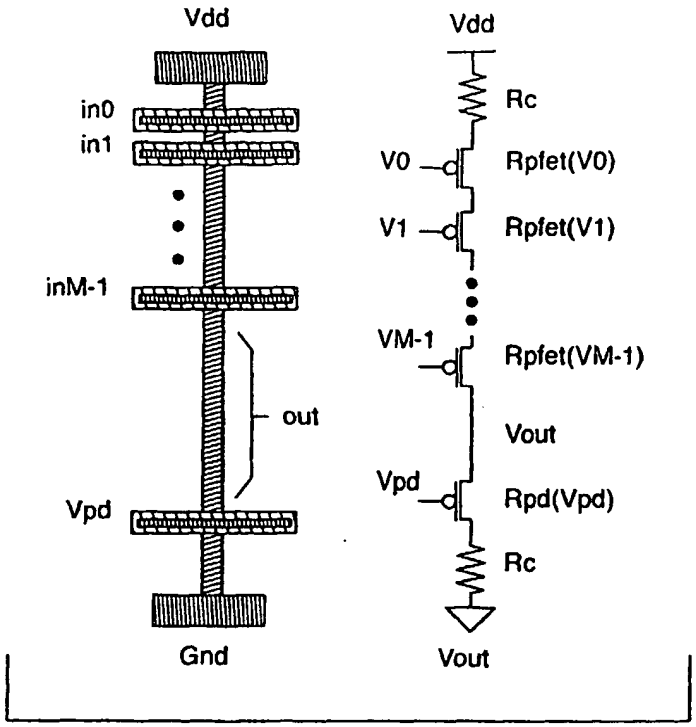
Vdd
in0
in1
inM-1
out
Vpd
Gnd
Vdd
Rc
V0
Rpfet(V0)
V1
Rpfet(V1)
VM-1
Rpfet(VM-1)
Vout
Vpd
Rpd(Vpd)
Rc
Vout

FIG. 5

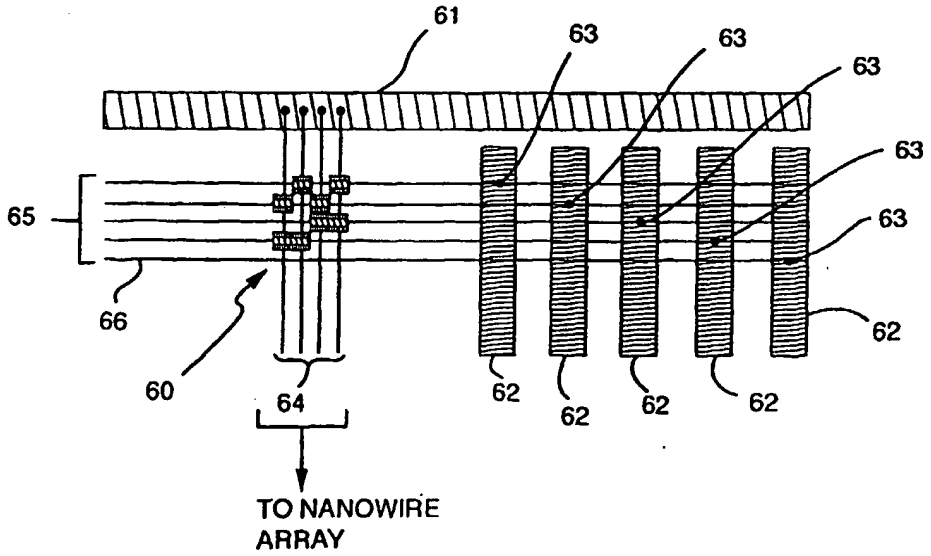
61
63
63
63
63
63
62
65
66
60
64
62
62
62
62
TO NANOWIRE
ARRAY

FIG. 6

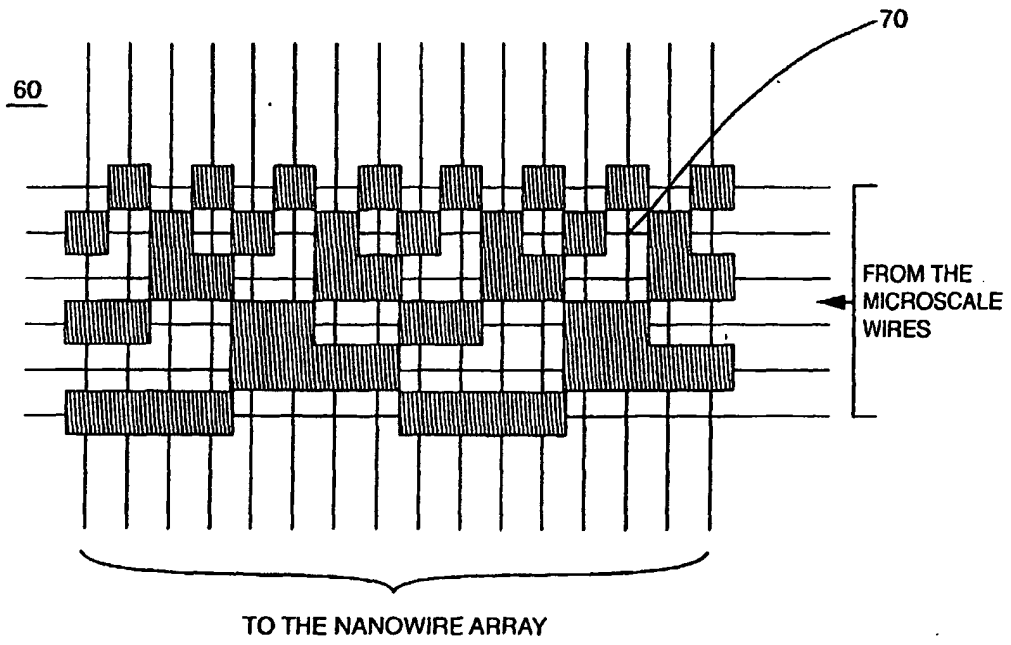

FIG. 7

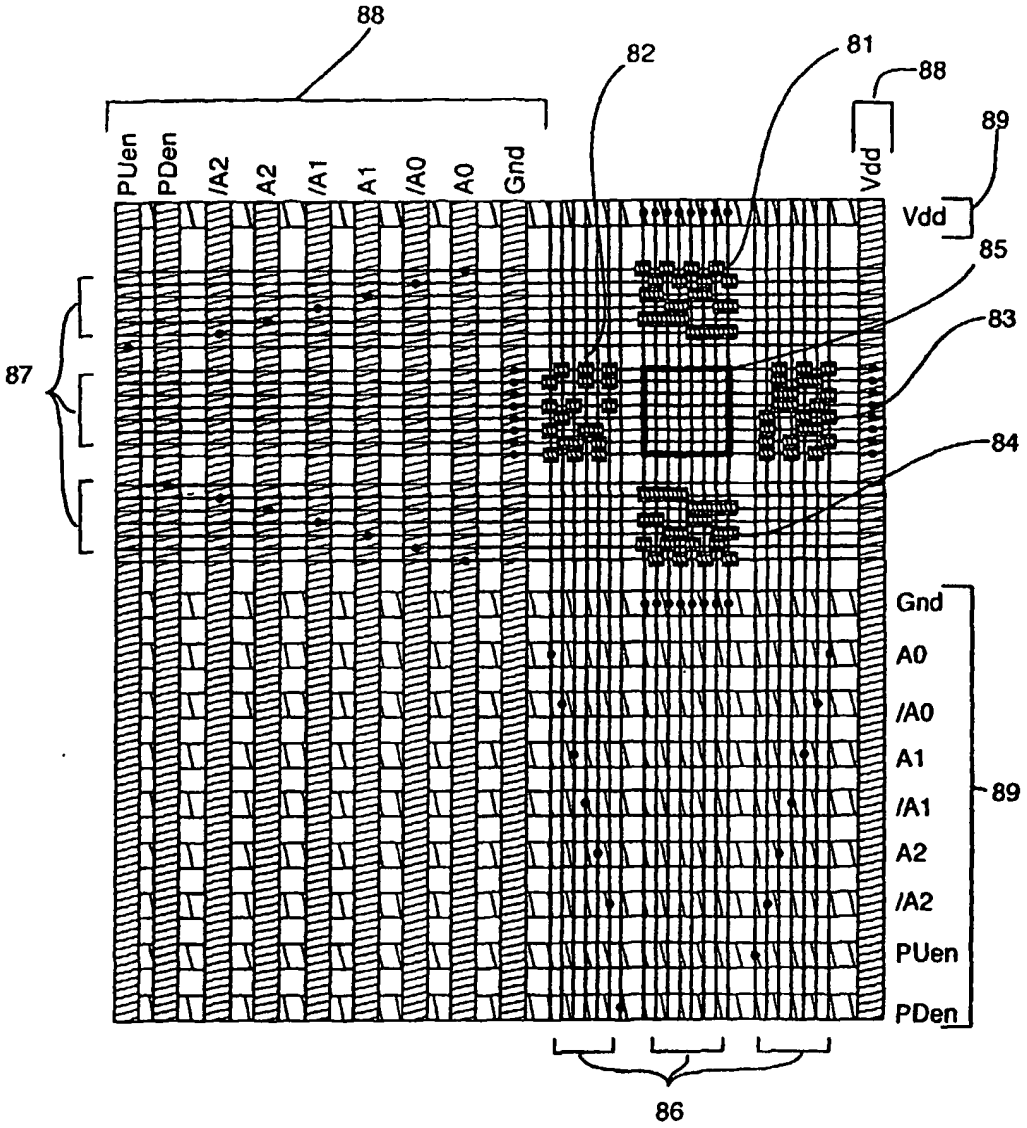
88
82
81
88
89
PUen
PDen
/A2
A2
/A1
A1
/A0
A0
Gnd
Vdd
Vdd
85
83
87
84
Gnd
A0
/A0
A1
/A1
A2
/A2
PUen
PDen
89
86

FIG. 8

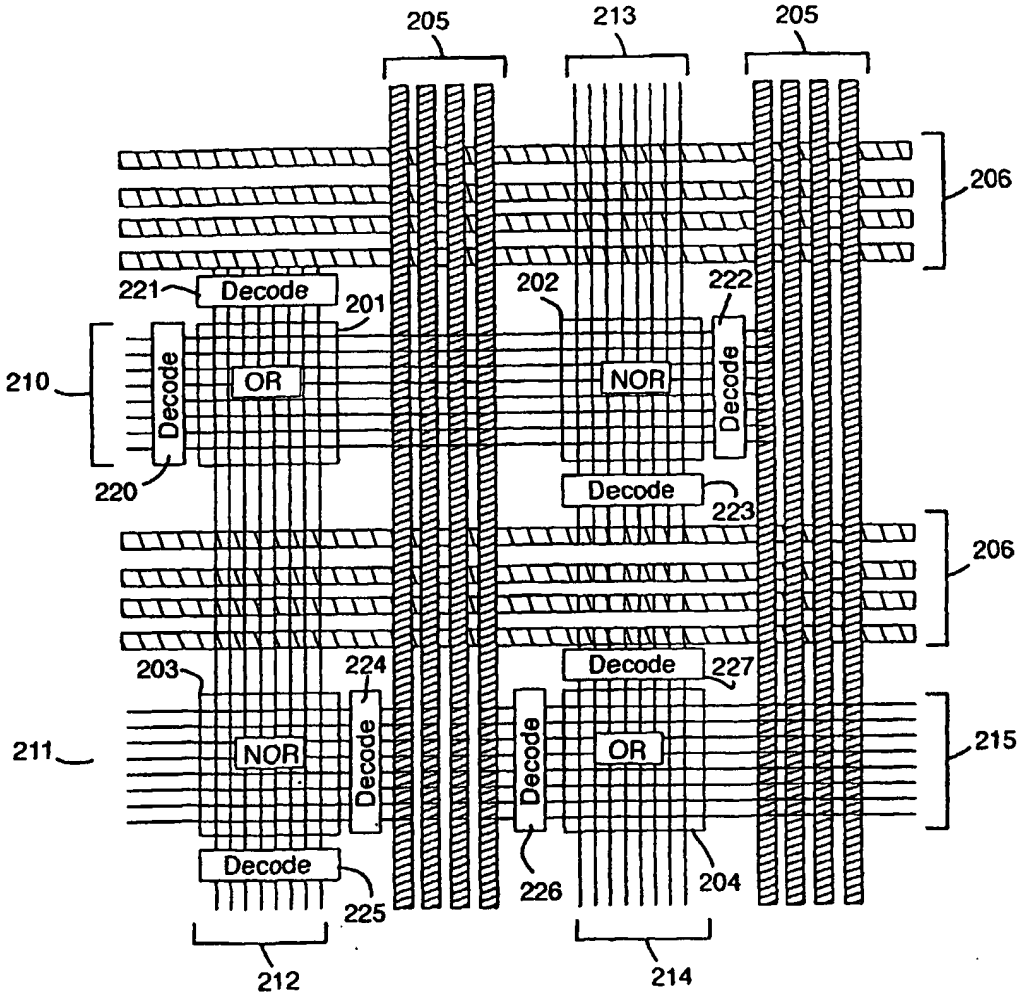
205
213
205
206
221
Decode
201
202
222
210
Decode
OR
NOR
Decode
220
Decode
223
206
203
224
Decode
227
211
NOR
Decode
Decode
OR
215
Decode
226
204
225
212
214

FIG. 9

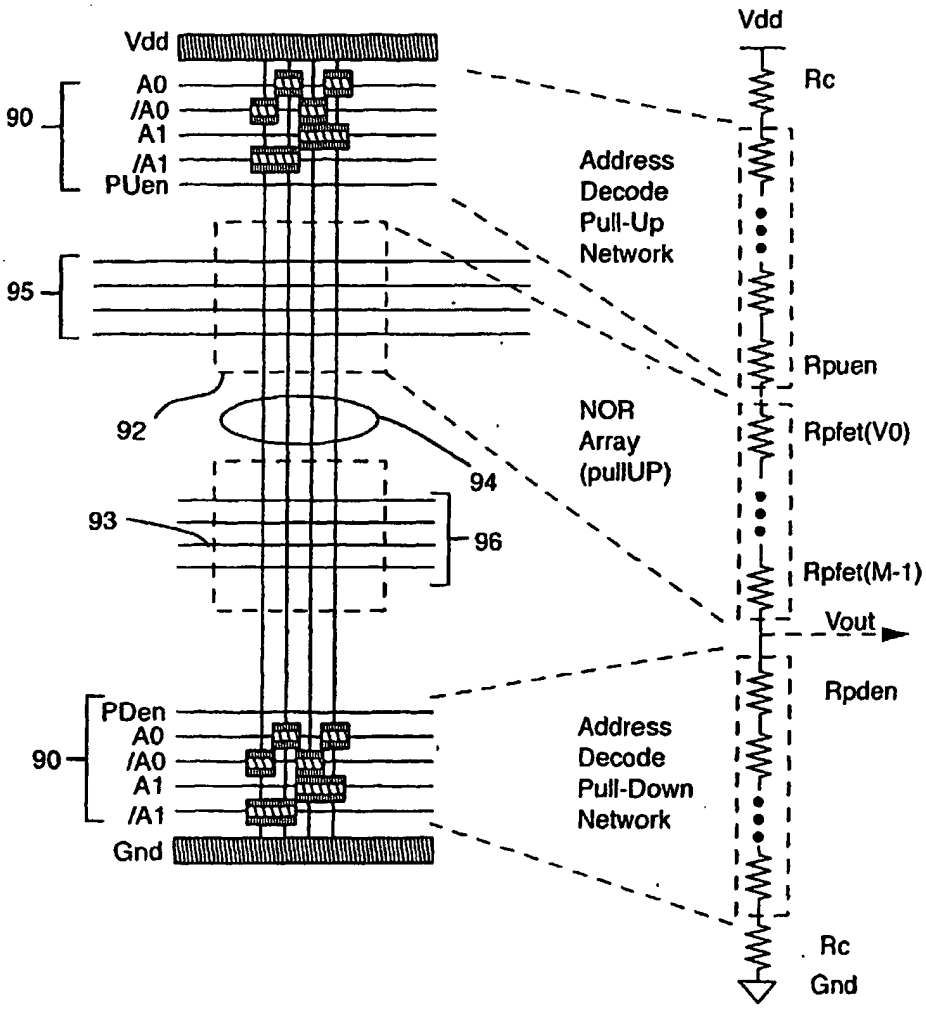
Vdd
A0
/A0
A1
/A1
PUen
90
95
92
94
93
96
PDen
A0
/A0
A1
/A1
90
Gnd
Address
Decode
Pull-Up
Network
NOR
Array
(pullUP)
Address
Decode
Pull-Down
Network
Vdd
Rc
Rpuen
Rpfet(V0)
Rpfet(M-1)
Vout
Rpden
Rc
Gnd

FIG. 10

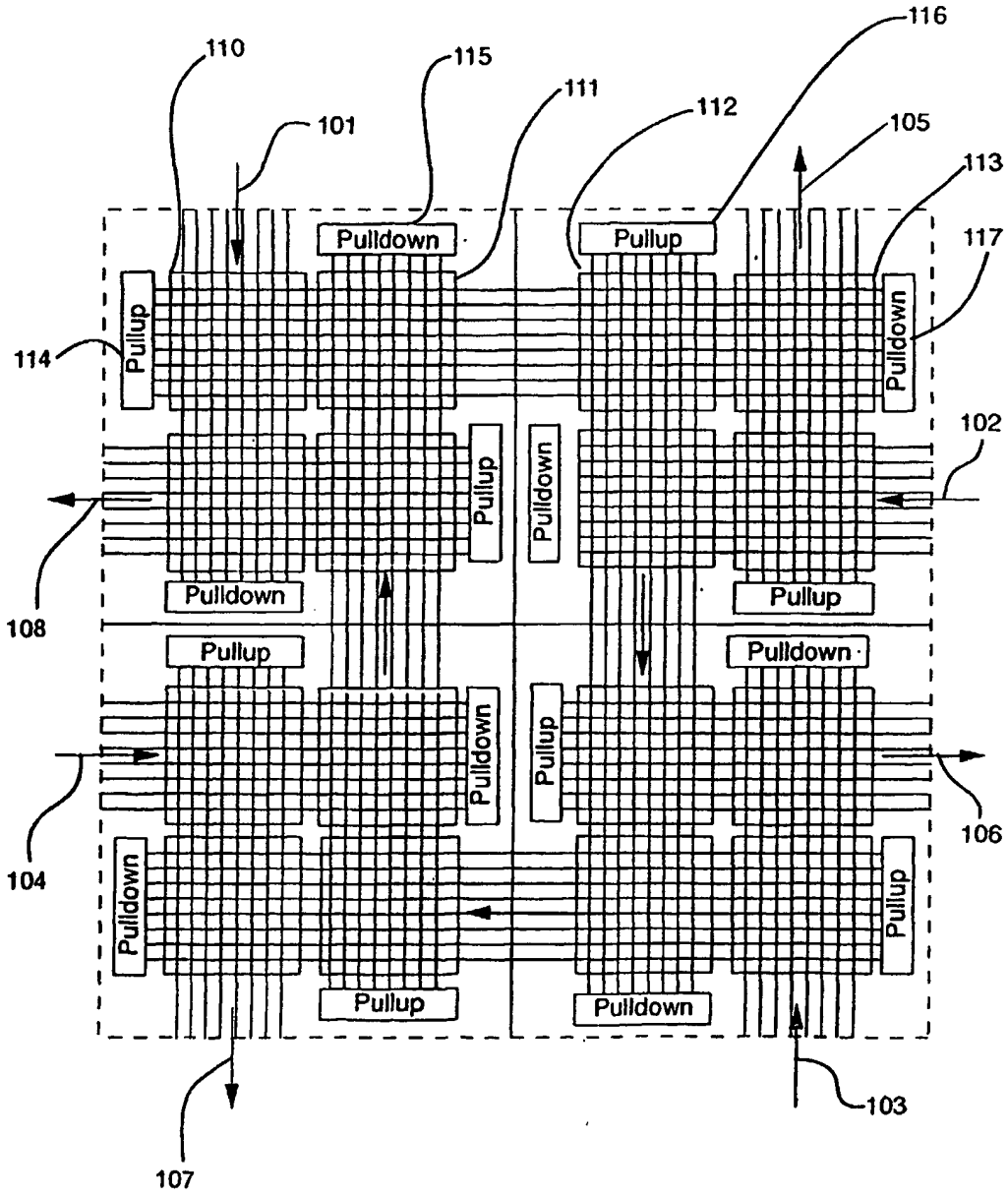
110
115
111
112
116
101
105
113
117
114
102
108
104
106
103
107
Pulldown
Pullup

FIG. 11

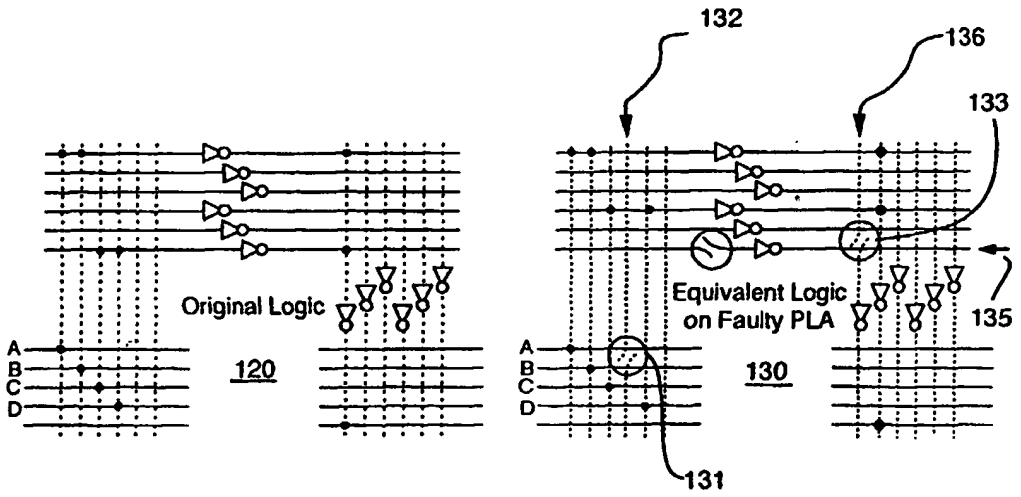
132
136
133
Original Logic
Equivalent Logic
on Faulty PLA
135
A
B
C
D
120
130
131

FIG. 12